Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SIXTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), MAY 2019

Course Code: EC304

Course Name: VLSI

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1 a) How electronic grade silicon is prepared from raw SiO_2? (5)

b) Illustrate the dry and wet oxidation technique used in IC fabrication with schematic diagram. (10)

2 a) With the help of mathematical equations, explain the distribution of impurities in a semiconductor in ion implantation process. (10)

b) Phosphorous is implanted in a p-type silicon sample with a uniform doping concentration of 5×10^{16} atoms per cm^3. If the beam current density is 2.5μA per cm^2 and the implantation time is 8 minutes, calculate the implantation dose and peak impurity concentration. Assume $\Delta Rp=0.3\mu m$ (5)

3 a) Explain N-well CMOS IC fabrication sequence with the help of neat diagrams. (10)

b) Explain one method of fabrication of capacitor structure in integrated circuits. (5)

PART B

Answer any two full questions, each carries 15 marks

4 a) Explain the various types of power dissipation in CMOS inverter? Derive the expression for total power consumption of a CMOS inverter. (10)

b) Why PMOS transistor can pass only strong ones and NMOS can pass strong zeros. (5)

5 a) Draw the circuit diagram and layout of a two input CMOS NAND gate. (10)

b) Implement the function u = A'B+AB' and v = AB+A'B' using complementary pass transistor logic. (5)

6 a) Explain the structure and working of a transmission gate. (10)
Implement 4×1 multiplexer using transmission gates.

b) Implement the function f = [AB + C (DE+F)]' using static CMOS logic. (5)

PART C

Answer any two full questions, each carries 20 marks

7 a) Explain the read and write operation of a six transistor CMOS SRAM cell. (10)

b) What is FPGA? Explain its constructional details with diagram. What are the advantages of FPGA? (10)

8 a) Design a 4-bit × 4-bit NOR-based ROM array and explain its working. (10)

b) Explain the read and write operation of a three-transistor DRAM cell. (10)

9 a) Explain the working a 16-bit carry-by pass adder and write down the expression (10)

for worst-case delay.

b) Explain 4×4 bit-array multiplier with block diagram. (10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SIXTH SEMESTER B.TECH DEGREE EXAMINATION(S), DECEMBER 2019

Course Code: EC304

Course Name: VLSI

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1 a) With a neat sketch, explain the process of ion implantation for IC fabrication. (8)

b) Draw schematic and explain any two CVD processes. (7)

2 a) With the help of neat diagram explain crystal growth in Czochralski process. (7)

b) Define photolithography and discuss various steps involved in photolithographic process. (8)

3 a) A Si sample is covered with 0.25µm thick SiO_2 layer. Find the time required to grow an additional 0.2µm thick SiO_2 at 1200□ by dry oxidation. For dry oxidation at 1200□ B = 0.045 µm, B/A = 1.120 µm/hr, τ = 0.027 (5)

b) Solve Fick's law for pre deposition diffusion. (3)

c) List various methods of resistor fabrication. (7)

PART B

Answer any two full questions, each carries 15 marks

4 a) The VTC of an inverter is given in Figure 1. (4)

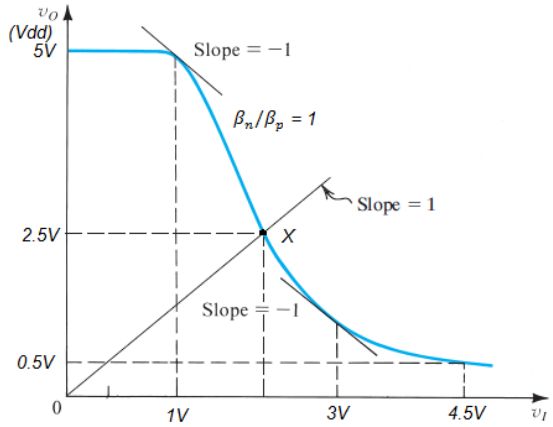

Figure 1.

Define the terms Noise Margin Low and Noise Margin High. Calculate their numerical values.

b) Calculate drain current for the region marked X in Figure 1. Given $V_{tn} = |V_{tp}| =$ $0.5V$ and $\beta_n = 1mA/V^2$. (3)

c) Draw the circuit of NMOS pass transistor logic. Discuss its output characteristics and comment on the drawbacks. (8)

5 a) For a two input CMOS NOR gate, draw (10)

i. Circuit diagram

ii. Stick diagram

iii. Layout

b) Implement the logic function **(AB + C(A+D))′** using CMOS logic. (5)

6 a) Draw the switching characteristics of CMOS inverter and discuss the terms associated with it. (6)

b) Realize an XOR gate using (9)

i. CMOS logic
ii. NMOS pass transistor logic
iii. Transmission gate logic

PART C

Answer any two full questions, each carries 20 marks

7 a) Draw the circuit diagram of a 6T CMOS SRAM cell. Briefly explain the read and write operations by drawing simplified models. (10)

b) Implement a full adder using complementary static CMOS. Explain the merits and demerits associated with the circuit. (10)

8 a) Draw and explain the internal architecture of an FPGA. List four applications of FPGA. (10)

b) With block diagrams, illustrate the behaviour of linear carry select adder and square root carry select adder. (10)

9 a) How does a sensing amplifier contribute to the operation of an SRAM? With a circuit diagram, explain how differential sensing is applied to an SRAM memory column. (10)

b) Show the conversion of a ripple carry adder into a carry bypass adder. Draw the block diagram of a 16 bit carry bypass adder and show the worst-case delay path. (10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Sixth semester B.Tech examinations (S), September 2020

Course Code: EC304

Course Name: VLSI

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1 a) What is annealing? Explain the various types. (5)

b) Illustrate with diagram, the principle of crystal growth by Czochralzki method and Float zone process. Compare these processes. (10)

2 a) Determine the ratio of silicon consumed to the thickness of grown SiO_2 layer over silicon wafer. If SiO_2 layer of 0.4 μm is to be grown, what would be the thickness of used up silicon. Molecular weight of SiO_2 = 60.08g.mole, density of SiO_2 =2.2g/cm^3 , atomic weight of Si =20.09 g.mole, density of Si =2.33g/cm^3 (5)

b) Derive and explain Fick's 1st and 2nd laws (6)

c) What are the steps involved in photolithography process. (4)

3 a) Explain N-well CMOS IC fabrication sequence with neat diagrams. (9)

b) With the aid of neat diagrams explain fabrication process of transistors (6)

PART B

Answer any two full questions, each carries 15 marks

4 a) Implement the following functions using pass standard CMOS logic (6)
i) y = a AND b ii) y = a XNOR b

b) Draw the circuit diagram, stick diagram and layout of a CMOS inverter. (9)

5 a) Explain pass transistor logic. What are its demerits and how it can be remedied? (8)

b) Explain the DC output characteristics of CMOS inverter and discuss various regions in the characteristics. (7)

6 a) List the various types of power dissipation in CMOS. Which type is dominant and why? (5)

b) Explain the significance of design rules. What are the different design rules in CMOS technology? (5)

c) Discuss transmission gates. Implement XNOR gates using transmission gate logic. (5)

PART C

Answer any two full questions, each carries 20 marks

7	a)	Explain three different designs of ROM using CMOS transistors.	(10)
	b)	With neat figures and appropriate equations, explain the design of Linear Carry Select adders.	(10)
8	a)	With neat block diagram explain 4×4 bit-array multiplier.	(10)
	b)	Draw the CMOS implementation of a NAND ROM cell to store 4 words of 4bits each which are as follows 1010, 1000, 1101 and 1001.	(10)
9	a)	Explain six transistor CMOS SRAM cell .What are its merits and demerits.	(8)
	b)	Compare carry bypass adder and carry select adders.	(6)
	c)	With diagram, explain how a voltage sense amplifier can read and write a bit.	(6)

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