Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Convert the following (8)

(i) $(AB6)_{16}$ to Decimal (iii) $(543.26)_{10}$ into Octal

(ii) $(247.36)_8$ into Hexa Decimal (iv) $(AF9.B0D)_{16}$ into Binary

b) Consider the signed binary numbers A = 01000110 and B = 11010011 where B is in 2's complement form. Find the value of the following mathematical expression (7)

(i) A + B

(ii) A - B

(iii) B - A

2 a) Hamming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Even parity (ii) Odd parity (8)

b) Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer (7)

$F(A, B, C, D) = \sum m (0, 1, 3, 5, 6, 7, 8, 9, 11, 13, 14)$

3 a) Minimize the following logic function using K- maps and realize using NAND gates alone (10)

$F(A, B, C, D) = \sum m (0, 3, 5, 8, 9, 11,15) + d (2, 3)$

b) Design a magnitude comparator to compare two 2-bit numbers $A = A_1A_0$ and $B = B_1B_0$ (5)

PART B

Answer any two full questions, each carries 15 marks.

4 a) Draw the circuit and explain the operation of TTL NAND gate (10)

b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and noise margin (5)

5 a) Implement the following function using PLA (8)

$F1(x, y, z) = \sum m (1, 2, 4, 6)$

$F2(x, y, z) = \sum m (0, 1 , 6, 7)$

b) Explain a MOD 6 asynchronous counter using J K Flip Flop (7)

6 a) Design a 3-bit synchronous counter using D Flip Flop (10)

b) Convert SR Flip Flop into J K Flip Flop (5)

PART C

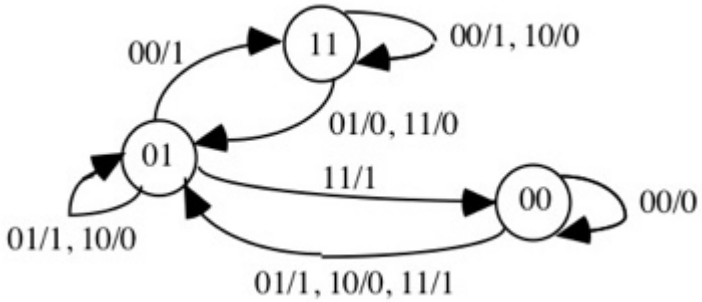
Answer any two full questions, each carries20 marks.

7 a) Draw the logic diagram of 3 bit PIPO shift register with LOAD/SHIFT control and explain its working. (10)

b) Explain Moore and Mealy machine models. Compare the models (10)

8 a) Draw the logic diagram of 3 –bit Johnson counter and explain the working with truth table. (10)

b) For the given state diagram, design a sequential circuit with D flip flops (10)



(i) Construct the state table.

(ii) Obtain the simplified input equations for all input flip flops and the simplified equation for the output.

9 a) Minimize the state table using implication chart. (10)

Present state	Next state		Output (Z_1Z_2)	
	X=0	X=1	X=0	X=1
0	0	1	00	00
1	4	2	00	00
2	7	1	00	00
3	2	6	01	10
4	6	5	10	00
5	3	4	01	11
6	1	6	01	10
7	3	8	10	00
8	8	7	01	11

b) Design a 101 sequence detector ,for overlapping case, using D Flip Flop (10)

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(S), MAY 2019

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks.

Marks

1 a) Convert the following numbers: (4)

(a) $(101111.1101)_2$ to decimal (b) $(53.625)_{10}$ to binary

b) What is the specialty of Grey code and specify how this property can be utilized in a practical application (4)

c) State the relationship between error detection ability, error correction ability and minimum distance of a code. An 8421 code is transmitted as Hamming code with even parity and the code received is 0011101. Determine the single error if any and correct it (7)

2 a) Obtain the minimal SOP expression for $\sum m(2,3,5,7,9,11,12,13,14,15)$ and implement it using NAND logic (7)

b) Using K-map, obtain the minimal sum of product of the following expression ABCD+AB'C'D'+AB'C+AB (8)

3 a) Obtain binary representation of $(-25)_{10}$ in (i) sign-magnitude (ii) 1's complement (iii) 2's complement form (5)

b) Derive expressions for the output of a 1-bit magnitude comparator and implement it using gates (10)

PART B

Answer any two full questions, each carries 15 marks.

4 a) Differentiate between PLA and PAL with necessary diagrams (7)

b) What is the significance of (a) propagation delay (b) power dissipation (c) Fan-out of gates. Compare CMOS, ECL and TTL logic families in terms of these parameters (8)

5 a) What is race-around condition in flip-flops? How is it solved? (5)

b) Design a mod-6 synchronous counter using T-flip-flops (10)

6 a) Draw the circuit of a TTL NAND gate with totem pole output. Mention the advantages and disadvantages of totem pole configuration (7)

b) Realize a J K flip-flop using D flip-flops (8)

PART C

Answer any two full questions, each carries20 marks.

7 a) Draw a serial input parallel output (4 bit) shift register. Convert this to a ring counter using suitable modifications (10)

b) Draw the block diagram of a finite state machine. Differentiate between Mealy and Moore machine with the help of block diagrams (10)

8 a) Design a 2 bit synchronous up/down counter using D flip-flop (10)

b) Reduce the following state table using implication chart method (10)

PS	NS, z	
	X=0	X=1
S0	S4, 0	S3, 1
S1	S5, 0	S3, 0
S2	S4, 0	S1, 1
S3	S5, 0	S1, 0
S4	S2, 0	S5, 1
S5	S1, 0	S2, 0

9 a) A clocked sequential circuit with single input X and single output Y produces output Z equal to 1, whenever the input X completes the sequence 110 and overlap is allowed. Obtain the state diagram and the minimum state table. Prepare excitation table and design the circuit using D flip-flop. (10)

b) List different classes of shift registers. Illustrate the use of the use of parallel LOAD/SHIFT in shift registers (10)

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks.

Marks

1 a) Two numbers A & B in Hex are given A= 85CA, B= 23C6 (10)

i. Find the Decimal equivalent of A & B

ii. Find the binary of A & B

iii. What is the sum of A& B in HEX

b) Write down the algorithm for BCD Addition. Find the sum of numbers 74998 and 38976 by BCD addition. Show the steps clearly. (5)

2 a Express f =AB + AC + C + AD + ABC + ABC in standard SOP form. (7)

b Using K map simplify the SOP function, and realize it using logic gates. (8)

$f(a,b,c,d) = \Sigma m\ (0,1,2,4,5,6)$, $d = \Sigma\ (3,7,14,15)$

3 a) Realize a XNOR circuit using NAND gate only. (6)

b) A logic circuit has our inputs A,B,C and D. A four bit input is fed with A as MSB and D as LSB. Design and implement a circuit such that the output is one when the input is more than or equal to decimal 6. (9)

PART B

Answer any two full questions, each carries 15 marks.

4 a) Realize a 3 bit gray to binary decoder using PROM. Give all details. (7)

b) What is meant by race around condition? How it is eliminated. Illustrate with the help of necessary sketches. (8)

5 a) Convert a JK flipflop into a D flipflop, (7)

b) Design and implement a circuit for generating the sequence 2-5-7-3-0 (8)

6 a) Define the following (4)

(i) Fan out

(ii) Fan in

b) What is the difference between a latch and a flipflop. (3)

c) Design an asynchronous 3 bit up counter. Write complete truth table and excitation table. (8)

PART C

Answer any two full questions, each carries20 marks.

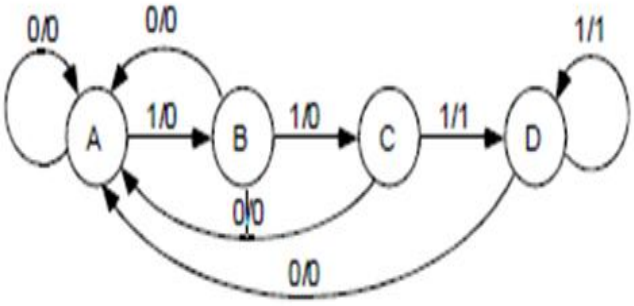
7 a) A register is to be designed, which provides all the following functions shift left, shift right, parallel in, parallel out, serial in, serial out, serial in parallel out and parallel in serial out. Draw the circuit for a 4 bit data (serial/parallel) and provide its working. (10)

b) Draw the Mealy machine for the given table. (10)

Present state	Next state, output	
	x=0	x=1
y_1 y_0	y_1 y_0 / z	y_1 y_0 / z
0 0	0 1, 0	1 0, 0
0 1	0 1, 1	1 0, 0
1 0	0 1, 0	1 1, 0
1 1	0 1, 0	1 1, 1

8 a) Draw the logic diagram of a Johnson counter. Why it is called a divide by 2N counter. Draw the neat diagram of clock and output waveforms of a 4 bit Johnson counter. (8)

b) Use the state reduction technique and implement the circuit for the given state diagram. (12)



9 a) Design a mealy machine to detect an input sequence10110. The system should be able to detect overlapped sequence. Also draw the state diagram (10)

b) Obtain a minimum row primitive flow table for the state table shown below. (10)

	X_1X_2				
	00	01	11	10	Z_1Z_2
1	(1)	7	-	4	11
2	(2)	5	-	4	01
3	-	7	(3)	11	10
4	2	-	3	(4)	00
5	6	(5)	9	-	11
6	(6)	7	-	11	01
7	1	(7)	14	-	10
8	(8)	12	-	4	01
9	-	7	(9)	13	01
10	-	7	(10)	4	10
11	8	-	10	(11)	00
12	6	(12)	9	-	11
13	8	-	14	(13)	11
14	-	12	(14)	11	00

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third semester B.Tech degree examinations (S) September 2020

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) i. Convert the hexadecimal number 2FC3 into binary and decimal. (5)

ii. Write down the Octal equivalent of hexadecimal number 3A2E.

iii. Subtract binary number 10110 from 10001001

b) Write down the 1's and 2's complement of the following numbers. (6)

i. – 4

ii. +253

iii. – 181

c) Determine the Hamming code for the information 1011, with even parity. (4)

2 a) Using the Boolean theorems simplify the following expressions. (8)

(i) $\boldsymbol{Y = \bar{A}C\overline{(\bar{A}BD)} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C}$

(ii) $\boldsymbol{Y = A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C}$

b) Using K map simplify the SOP function, and realize it using only NAND gates. (7)

f(a,b,c) = Σm (0,2,3,4,5,6)

3 a) Realize a 2 bit comparator. (7)

b) Implement the following function using an 8 X 1 MUX. (8)

F(A,B,C,D) = Σm (1,3,4,11,12,13,14,15)

PART B

Answer any two full questions, each carries 15 marks.

4 a) List any four performance ratings of TTL family. (4)

b) Draw the circuit of a CMOS inverter and explain its working (4)

c) Explain the working of a master slave JK flipflop, with the help of circuit diagram. (7)

5 a) Explain the working of a 3 bit UP/DOWN counter. (7)

b) Implement the following two Boolean functions with a PLA: (8)

F1(A,B,C) = Σm (0,1,2,4)

F2(A,B,C) = Σm (0,5,6,7)

6 a) Describe the working of a 3 bit TTL NAND gate in totem pole configuration. (8)

b) Convert a D flipflop into a JK flipflop, showing all the steps. (7)

PART C

Answer any two full questions, each carries 20 marks.

7 a) Explain the working of a 4 bit PISO register. Draw the circuit and timing diagram. (10)

b) Draw the Moore sequential model. How it differs from Mealy machine. (5)

c) For the Mealy Model State table is given below draw the state diagram. (5)

PS		NS				O/P	
		X=0		X=1		X=0	X=1
Y1	Y2	Y1	Y2	Y1	Y2	Z	Z
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

8 a) Explain the working of a 4 bit twisted ring counter, with the help of timing diagrams. (10)

b) For the state tables of the machines given below, find the equivalence partition and a corresponding reduced machine. (10)

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,1	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

9 a) Draw the state diagram, state transition table and state equation using D flip flop for the given state table. (10)

PS	NS		O/P	
	X=0	X=1	X=0	X=1
A(00)	A	B	0	0
B(01)	C	B	0	0
C(10)	A	D	0	0
D(11)	C	B	1	0

b) Design a synchronous counter using T flipflop to count the following sequence. (10)
0-3-1-4-6-0

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