Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: EC 206

Course Name: COMPUTER ORGANIZATION

Max. Marks: 100 Duration: 3 Hours

PART A (MODULE I & II)

Answer any two out of three questions Marks

1	(a)	How is Carry- Look ahead Adder different from Ripple Carry Adder? Explain with relevant diagrams and write down the delay equations for both adders.	(10)
	b	In a 32- bit Adder circuit assume each 2 -input gate delay is 200ps. Calculate (a) Total delay for a Carry Look Ahead adder when the full adder delay is 400ps and is divided in to 4 bits block (b) Total delay for a Prefix Adder.	(5)
2	a	Design a 16-bit prefix adder and explain its working. Also obtain the delay of an N-bit prefix adder	(10)
	b	What is meant by R-Type instruction? Draw the R-Type machine instruction format. Find the machine code for the R-Type instruction add ***$s0,$s1,$s2*** with function code 32.	(5)
3	a	Design a 4-bit right and left shifter using multiplexers.	(5)
	b	What are I-Type instructions ? Explain with its instruction format.	(5)
	c	Explain the MIPS assembly codes for conditional branch instructions ***beq*** and ***bne*** with examples.	(5)

PART B (MODULE III&IV)

Answer any two out of three questions.

4	a	Discuss the different MIPS addressing modes.	(8)
	b	What are Pseudo instructions? Given the pseudo instruction " mov $s1,$s2 ". Write down its corresponding MIPS instruction and explain its working.	(7)
5	a	Describe step by step the working of a single cycle data path for subtracting two numbers.	(10)
	b	What are the parameters used for the performance analysis of a single cycle processor? Explain.	(5)

6	a	Draw and explain the working of complete MIPS multi cycle processor using an example.	(10)
	b	What are the steps involved in translating a high level language program into a machine language program ?	(5)

PART C(MODULE V&VI)

Answer any two out of three questions. Each carries 20 marks

7	a	A program has 2000 data access instructions (loads or stores), and 1250 of these requested data values are found in the cache. The other 750 data values are supplied to the processor by main memory or disk memory. What are the miss and hit rates for the cache?	(5)
	b	What is virtual memory ? Explain the process of address translation.	(5)
	c	Differentiate between programmed I/O and interrupt driven I/O.	(5)
	d	How is SRAM different from DRAM?	(5)
8	a	Explain the principle of Cache memory. What are the different cache mapping techniques? Discuss in detail.	(10)
	b	What is page table and how is it useful in address translation?	(5)
	c	Explain DMA.	(5)
9	a	Why standardisation of input/output interfaces is necessary? Explain PCI, SCSI and USB.	(8)
	b	Explain the memory system hierarchy. Draw and explain the internal organization of a memory chip.	(7)
	c	What are the various write policies used in cache?	(5)

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION(R&S) MAY 2019

Course Code: EC206

Course Name: COMPUTER ORGANISATION (EC)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1	a)	Explain Propagate adder and ripple carry adder.	(8)
	b)	Illustrate the use of shifters and rotators with example in arithmetic circuits.	(7)
2	a)	Define the following terms of MIPS processor: (i) Register Set. (ii)Operands.(iii) Memory. (iv) Registers.	(8)
	b)	With example explain briefly R-type and I-type Instruction format in Machine Language.	(7)
3	a)	Define fixed point number systems with examples.	(7)
	b)	Convert to MIPS assembly instruction (i) 0x2128FF6A (ii) 0x0253882A	(8)

PART B

Answer any two full questions, each carries 15 marks

4	a)	Explain Pseudoinstructions and exceptions in MIPS.	(8)
	b)	Explain Floating Point instructions used in MIPS	(7)
5	a)	Briefly define the state elements used in MIPS processor.	(7)
	b)	Explain the data path of single cycle R-type instruction.	(8)
6	a)	With neat diagram explain multi cycle control for R-type instruction.	(8)
	b)	Explain signed and unsigned instructions used in MIPS	(7)

PART C

Answer any two full questions, each carries 20 marks

7	a)	Illustrate the different modes of data transfer in I/O systems.	(5)
	b)	Mention the working of memory cells SRAM and DRAM.	(10)
	c)	Draw Memory Hierarchy diagram.	(5)
8	a)	Explain Address Translation in virtual Memory.	(8)
	b)	With neat diagram explain briefly TLB.	(7)
	c)	Define Write through and Write Back Policies.	(5)
9	a)	Illustrate the different mapping methods of Cache Memory.	(8)
	b)	Write short notes on Segmentation and paging.	(7)
	c)	Sketch the internal organization of a memory chip.	(5)

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION(S), DECEMBER 2019

Course Code: EC206

Course Name: COMPUTER ORGANISATION

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks

			Marks
1	a)	Explain with neat diagram a 32 bit ripple carry adder.	(3)
	b)	With neat diagram explain Arithmetic Logic Unit	(5)
	c)	Explain the R- type instruction format of MIPS with example	(3)
	d)	Translate the following machine language code into MIPS assembly language: 0xAD310004	(4)
2	a)	Design a 4×4 binary multiplier. Illustrate with an example	(7)
	b)	Write notes on MIPS register set.	(4)
	c)	Translate the following MIPS assembly code to MIPS machine language code in hexadecimal form: lw $t2, 32 ($0)	(4)
3	a)	Explain how floating point numbers are represented in computer's memory.	(6)
	b)	Differentiate Big-Endian and Little-Endian machines	(4)
	c)	Explain load word and store word instructions with examples	(5)

PART B

Answer any two full questions, each carries 15 marks

4	a)	With examples, explain the different addressing modes available in MIPS.	(10)
	b)	Explain the control unit of a multi cycle processor	(5)
5	a)	Explain the various steps for executing a program	(9)
	b)	What are the weaknesses of a single cycle processor. How are they eliminated in a multi cycle processor?	(6)
6	a)	What are exceptions ? How the exceptions are handled ?	(7)
	b)	Draw and explain datapath for single cycle implementation for R-type instructions.	(8)

PART C

Answer any two full questions, each carries 20 marks

7	a)	With the help of a diagram, explain the concept of memory hierarchy.	(5)
	b)	Distinguish between Programmed I/O and Interrupt driven I/O	(5)
	c)	Explain how a virtual address is translated into a physical address in virtual memory using page table.	(10)
8	a)	Differentiate between SRAM and DRAM	(6)

	b)	Write short notes on (i) Serial port (ii) Parallel port	(4)
	c)	Explain LRU replacement algorithm	(4)
	d)	Explain with diagram direct mapping method in cache memory.	(6)
9	a)	What is meant by ROM? Explain the various types of ROM	(5)
	b)	With the help of a circuit diagram, explain the working of a SRAM cell.	(5)
	c)	Explain the concept of cache memory. Also define Miss Rate, Hit Rate and Average memory access time.	(10)

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth semester B.Tech examinations (S), September 2020

Course Code: EC206

Course Name: COMPUTER ORGANISATION (EC)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1 a) Draw the block diagram of a 16-bit ripple carry adder using full adders. Calculate the delay of a 32-bit ripple carry adder. Assume a full adder delay is 200ps. (7)

b) Express the following base 10 numbers in 16-bit fixed-point two's complement format with eight integer bits and eight fraction bits. Express in IEEE 754 single-precision floating-point format also. Express your answer in hexadecimal. (8)

(a) -20.5 (b) 24.25

2 a) Explain any two assembly instruction formats in MIPS with examples. (6)

b) Write the operation performed in MIPS processor when it executes the following instructions (9)

(a) add $t0, $s4, $s5
(b) lw $t2, 32($0)
(c) sw $s1, 4($t1)

3 a) Draw the symbol and implementation of a 4 x 4 multiplier. (7)

b) Discuss about operands and registers of MIPS processor. Write the use of $0, $gp, $sp and $t8. (8)

PART B

Answer any two full questions, each carries 15 marks

4 a) Explain five addressing modes of MIPS with example. (15)

5 a) Draw the datapath for single cycle processor for *sw* instruction. (9)

b) List the characteristics of single-cycle and multi cycle microarchitectures. (6)

6 a) How does a multicycle processor address the weakness of single-cycle processor? (7)

b) Explain the steps involved in executing a high level language program. Draw the flow chart. (8)

PART C

Answer any two full questions, each carries 20 marks

7	a)	Explain any two modes of data transfer between the processor/memory and I/O devices in a computer system.	(6)
	b)	Draw the internal organization of a DRAM cell and explain the read and write operation.	(6)
	c)	Illustrate virtual address to physical address translation using page table.	(8)
8	a)	Define miss rate and average memory access time.	(6)
	b)	Draw the internal organization of a SRAM cell and explain the read and write operation.	(8)
	c)	Compute the size of a 4096-word x 32-bit memory array. Also find the width of address and data bus.	(6)
9	a)	Describe temporal locality and spatial locality with respect to cache memory.	(6)
	b)	Illustrate how data is found in a C=8 word, 2-way set associative cache	(10)
	c)	Draw the internal organization of a 4 x 3 memory array.	(4)

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